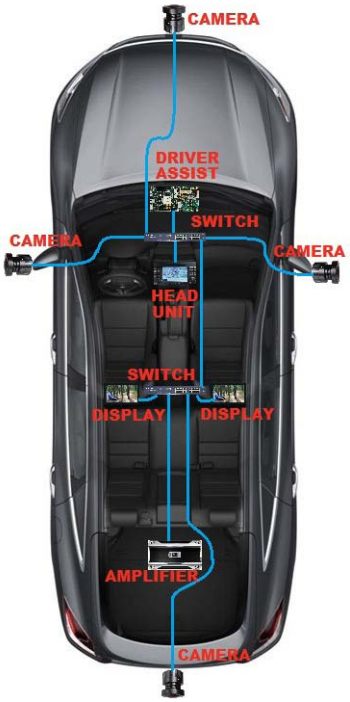
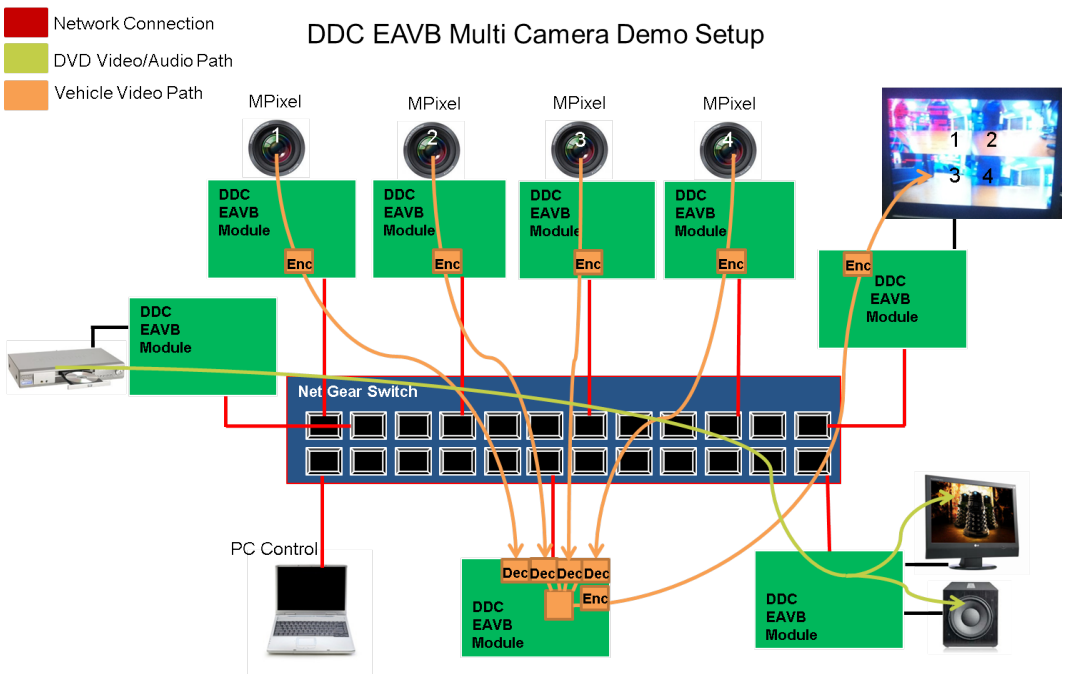
Ethernet Audio Video Bridging



The DDC EAVB IP Suite, running on Xilinx ® Spartan®-6 FPGA technology, collectively encompasses all of these standards – providing a complete solution for presenting and receiving audio and video media on a reliable and efficient AVB enabled network.

With recent consumer demand driving a continual increase of audio and video features in automobiles, innovation in cars today increasingly depends on the reliability of in-car networks. The amount of cabling required for using point-to-point connections with next-generation Infotainment, driver assist, and/or connected services is quickly becoming financially and mechanically impractical. Ethernet Audio Video Bridging (EAVB) is currently being standardized within IEEE to enable reliable, low-latency audio and video transmission within Ethernet subnets. The standards include 802.1AS, 802.1Qat, 802.1Qav, and 1722, which respectively define precise timing/synchronization protocol (PTP), media stream reservation protocol (MSRP), forwarding and queuing for time-sensitive media streams, and transport protocol for media streams.



The DDC EAVB demonstration system is comprised of multiple cameras and AV devices.

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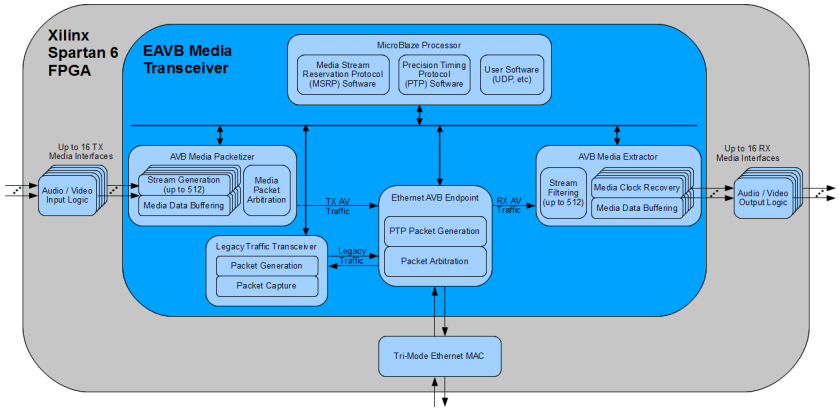
IP Core Solution



Ethernet AVB Endpoint

The Ethernet AVB Endpoint enhances standard Ethernet MAC functionality by providing prioritized arbitration of AV Ethernet traffic and legacy Ethernet traffic. The Endpoint additionally implements IEEE P802.1AS Precise Timing Protocol (PTP) using the Best Clock Master Algorithm (BMCA) and providing Real-Time Clock (RTC) timestamp information for transmitted packets. The Endpoint supports full clock master functionality and clock slave functionality of PTP, and implements bandwidth policing. The core functionality is implemented as a combination of a software driver and a logic netlist.

AVB Media Extractor

The AVB Media Extractor captures IEEE P1722 packets based on a programmable Stream ID filter, and routes the packet data to various media outputs. Up to 512 streams can be routed to up to 16 asynchronous media interfaces. The Extractor additionally uses timestamp information embedded in packets to recover the media clock of a given stream. The timestamp information is also used to present media data with the recovered media clock to downstream audio/video logic - providing a mechanism for synchronization of multiple forms of media across the AVB network.

AVB Media Packetizer

The AVB Media Packetizer forms IEEE P1722 EAVB packets based on software-programmable memory and incoming audio/video data from a number of media inputs. Up to 16 media interfaces are supported, and up to 512 streams can be generated from each media interface. The header contents and payload size of each stream is programmable through the software interface. Payload data of each media interface is buffered internally, and characterized by input media timing signals. Packets from each media interface are then sent to the Ethernet AVB Endpoint in a round-robin fashion at the start of every transmission cycle.

Legacy Traffic Transciever

The Legacy Traffic Transceiver contains buffers and logic for managing non-prioritized Ethernet traffic. Outgoing traffic from the MicroBlaze™ processor (e.g. MSRP, UDP, etc) is stored in a transmit buffer until the legacy traffic transmit window is open, and the AVB Endpoint accepts the packet. Incoming traffic from the Endpoint is stored in a receive buffer until the Microblaze processor reads the contents - a sequence that is initiated by an interrupt to the processor.

About Us

DDC is one of the most advanced FPGA houses in the United States. Staffed by over 30 engineers, over half of whom have advanced degrees, DDC has implemented some of the most advanced high performance algorithms in hardware. In some projects, DDC has translated C code to HDL and created small form factor embedded solutions that can outperformed supercomputers. The massively parallel architecture of FPGA requires deep expertise to optimize performance.

DDC has a long standing collaborative relationship with Xilinx as a leading Alliance Program Member providing Design Services, System Integration and Intellectual Property. DDC EAVB services include many possible customizations. DDC is part of the AVnu™ Alliance to help standardize EAVB. Our leading engineers will help you build on this platform to maximize the performance of your application.

AVNU™

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EAVB Development Kit

The design includes the following FPGA evaluation EAVB cores: EAVB Endpoint, AVB Media Packetizer, AVB Media Extractor (with media clock recovery), Ethernet Legacy Frame Capture and Ethernet Legacy Frame Generator.

Also included in the kit:
1) Two EAVB PCBs with a Xilinx® Spartan® -6 XC6S-LX75 FPGA, Marvell 88E1111 Ethernet PHY, 512 MB of Micron DDR2 SDRAM, 256Mb of FLASH memory
2) Two EAVB Audio/Video Mezzanine PCBs with an Audio CODEC, NTSC Decoder, and DVI output
3) Two 12V Power Supplies
4) One CAT5 Ethernet cable.

The kit will not include:
1) Xilinx® EDK (the DDC system will work without this software, but access to parameters via a GUI is only possible with the Xilinx EDK).
2) Video/Audio source –DVD player.
3) DVI Enabled monitor.
4) Speakers. DDC is also willing to work with clients to provide them a development kit with additional sensors if needed.

The kit is $9,999.99 and DDC is willing to work with clients to provide them a development kit with additional sensors if needed. DDC can also provide consulting time to work with you on development and integration, including other embedded electronics, and vehicular and driver-assist applications.

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