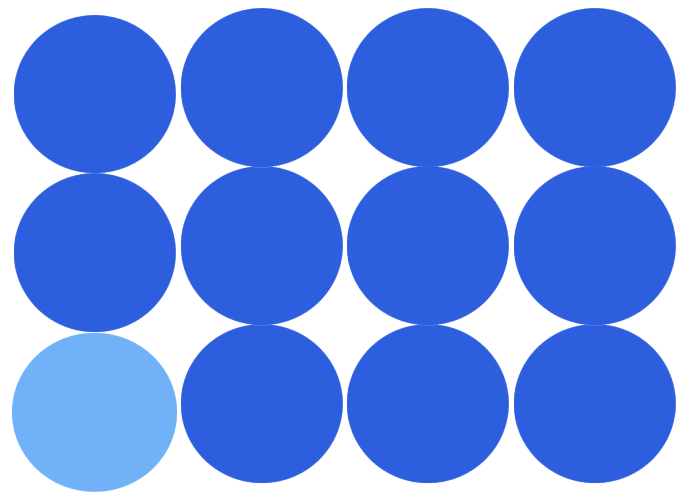


# SDRAM Controller Core Datasheet



Digital Design Corporation

## Features

- 360 Altera LEs
- >133MHz in slowest Stratix devices and Virtex II devices
- Field tested and proven
- Single cycle, and burst lengths of up to a full SDRAM row in length are supported.
- Internal/external auto refresh timer option
- Configurable, row, column, and, bank sizes.
- Easily integrated, easy place/route

**The SDRAM core is full featured core that has been field tested countless times.**

## General Information

The SDRAM core is full featured core that has been field tested countless times. It has generally been applied to video and frame buffer applications where there has been a need to burst data at a high rate into and out of memory (for video applications transferring high resolution images at 60 frames/second). The core automatically can burst across 4 banks for maximal transfer rate of lines (without doing page crosses). It is very flexible and configurable to optimize all possible bandwidth parameters.

The core has a simple command interface – Supply burst length, logical start address, command type, and a go pulse. The module pulses a “finished” signal to indicate completion. It supplies the FIFO/Memory read and write strobes sent to the system to time the data movement. The core supports automatic and completely transparent command splitting for bursts that cross a row boundary, freeing the designer from worrying about scheduling 2 commands. Eases issues related to packing images in memory. It also handles Master/Slave capability if operating in a system where 2 SDRAM controllers share the same memory. In slave mode the SDRAM controller will remove itself from the bus after the operation is complete and will never attempt an auto refresh cycle.

## Applications

- Video applications
- Image processing applications
- General applications

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