Graphics Engine Datasheet

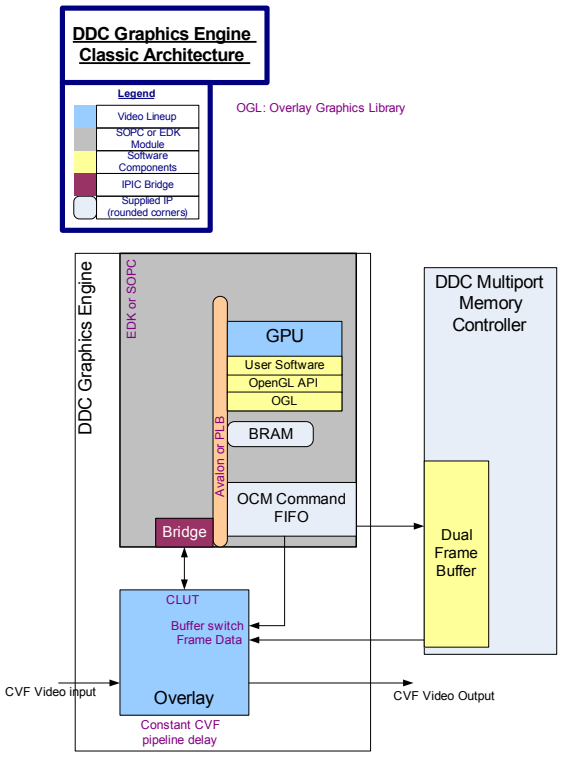
Features

- Overlay module with alpha blending of graphics data with another video stream
  - Index or full 32-bit color
  - Interfaces with DDC Multiport DDR Controller
  - Operates in RGB, color space converters available
- Floating Point Matrix Engine
  - Provides 3x3 or 4x4 floating point matrix multiplication
  - 32-deep Modelview matrix stack
  - Batch vertex transforms
- Rasterizer
  - Bresenham line-draw engine
  - Anti-aliasing polygon engine
- Per-Fragment Operations
  - Processes line draw commands
  - Can fetch frame buffer contents for alpha-blending draw operations
  - Parallel blending operation at full DDR rate
  - Basic texture support (no transforms)
- GPU
  - Microblaze or NIOS II
  - Executes DGEL commands
  - Makes use of accelerator modules where available
- PC Emulation
  - Environment allows debugging of graphics applications on a PC
  - Matches hardware operation

The DDC Graphics Engine is a combination of firmware and hardware implemented in an FPGA, which provides graphics drawing capabilities for embedded applications.

General Description

The Graphics Engine consists of several components: A system-on-chip module provides an embedded processor for executing graphics rendering functions; Hardware modules for acceleration and interaction with the frame buffer in DRAM; Video Overlay hardware allows a graphics scene to be blended with another video source. In addition to interacting with the Graphics Engine directly via the DDC Graphics Engine Library (DGEL), DDC's OpenGL implementation is available. Supported functions include 2D floating point primitives, matrix transformations with stack, alpha blending, stroke fonts and bitmaps.



Digital Design Corporation

Digital Design Corporation • 3820 Ventura Dr. Arlington Hts. IL 60004 • Phone: 847-359-3828 • Fax: 847-359-5418
Website: www.digidescorp.com • E-Mail: sales@digidescorp.com

Resources

Preliminary Resource consumption for Xilinx Virtex 5. Note that in addition, a DDR controller and video input and output blocks would be required. The full profile suports floating point coordinate spaces and matrix transformation of primitives, including a 32-deep matrix stack, and the hardware rasterizer. The limited profile does not include this support. Resource requirements for 720x480 video frame. Per-Fragment sizing is for 64-bit wide DDR interface, blending two pixels per clock (for instance, 9 DSP48s required per 32 bits of DDR data width).

Table 1: Full Profile Resource Requirements – Virtex5

Component	Slices	Flip-Flops	LUTs	36K BRAM	DSP48E
Microblaze	1331	1964	2108	program mem	5
Timer	184	295	263	0	0
Matrix Engine	1387	1878	2932	1	5
Rasterizer	1419	2475	3621	6	10
Per-Fragment Operations	1318	2357	2387	18	18
GPU_EDK total	**5639**	**8969**	**11311**	**25 + program mem**	**38**
Overlay	266	402	416	2	6
Graphics Engine Total	**5905**	**9371**	**11727**	**27 + program mem**	**44**

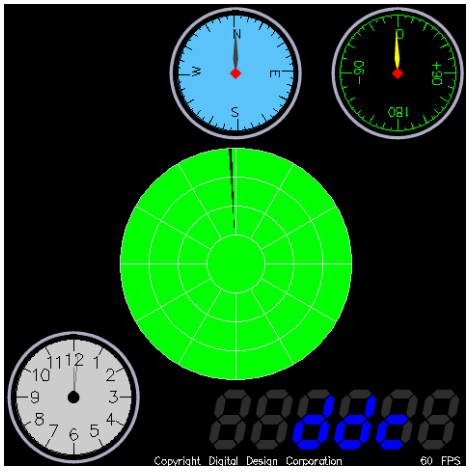
Table 2: Limited Profile Resource Requirements – Virtex5

Component	Slices	Flip-Flops	LUTs	36K BRAM	DSP48E
Microblaze	857	1245	1056	program mem	3
Per-Fragment Operations	624	1191	1261	4	16
Timer	184	295	263	0	0
GPU_EDK total	**1665**	**2731**	**2580**	**4 + program mem**	**19**
Overlay	266	402	416	2	6
Graphics Engine Total	**1931**	**3133**	**2996**	**6 + program mem**	**25**

Performance

This scene can be rendered in 8.2 ms with a 150 MHz Graphics Engine Clock:

- Circle polygons for clock face and upper gauge faces
- 7-segment display made up of transformed 6-sided anti-aliased polygons
- Radar made up of many triangle segments
- Text rendered with stroke fonts

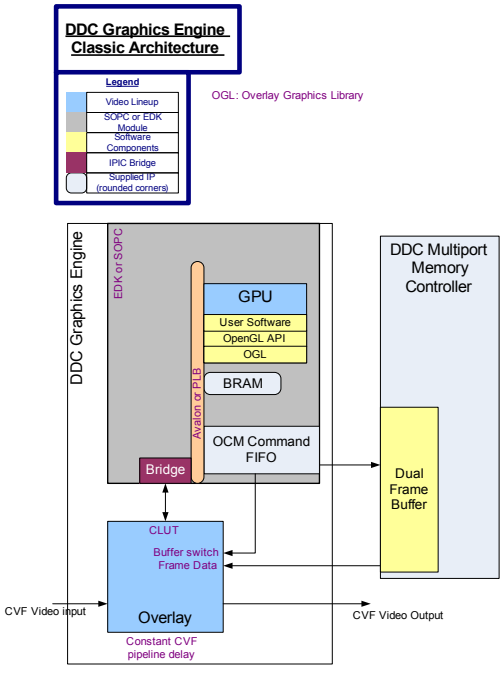


Clear time is dependent on DDR bandwidth.

Dual Core Architecture

The Graphics Engine Dual-core architecture (under development) allows graphics processing to be offloaded to the GPU, allowing the CPU to carry out other computational tasks.

- dgeLink library transforms DGEL functions into LocalLink or Atlantic packets (the com mand channel)
- Command channel may be within one FPGA, or bridged between devices, for ex ample over PCIe.



3820 Ventura Dr.
Arlington Heights IL, 60004
Phone: 847-359-3828
Fax: 847-359-5418
www.digidescorp.com
Email: sales@digidescorp.com

For more information contact Digital Design Corporation sales at:

+ 1-847-359-3828

or go to our website at:

www.digidescorp.com

Digital Design Corporation