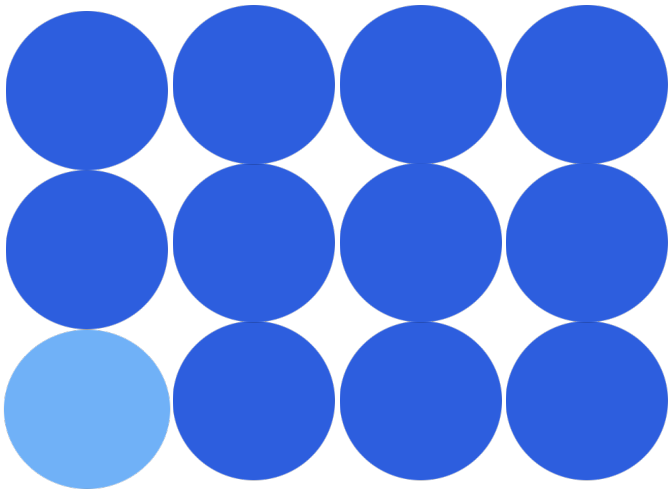
The J1850 Core Datasheet



Features

- SAE J1850 compatible
- Suitable for on- and off-road vehicle internal communications
- Fully synchronous (single system clock)
- Supports PWM and VPW modes of operation
- Automatic IFR generation
- Automatic message retry
- TX and RX buffering
- Generic feature control, synthesize only the features needed (for area savings)
- Behavioral model available for verification
- Test benches available for verification and example of operation

The J1850 Core is a full featured core that is compatible with the J1850 Serial Data Communications Protocol, an SAE class 2 protocol suitable for on and off-road land vehicles.

The J1850 Core

The design package consists of a core that contains the J1850 data specific functions for the operation of the core. The core supports both PWM and VPW modes of operation, allowing data rates of 41.6 Kb/s and 10.4 Kb/s respectively. An external transceiver chip is required to drive a J1850 bus at the proper voltages, as they are beyond the output capabilities of FPGAs.

J1850 uses CSMA/CR arbitration, which allows non-colliding transmission without a bus master. The core will listen for the specified listening period before beginning transmission, after which a collision resolution scheme based on message prioritization is used to resolve multiple simultaneous transmissions. The J1850 core will cease transmission if it has a lower priority than another J1850 node on the bus.

The core includes both transmit and receive paths, and the ability to automatically dispatch an In-Frame Response (IFR) data field, when an IFR is requested by received frame. This is done without requiring servicing by the SOC controller.

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The J1850 Core Design

FIFOs are provided for both the transmit and receive paths, to allow the SOC host controller to queue multiple transmissions to the J1850 bus, and allow for delay if the core must wait for bus priority. This functionality is provided through use of a command code which allows the interpretation of the written byte as header information, address, or data bytes. If the core looses an arbitration, it waits until the quiet period is satisfied and retries the transmission automatically. Similarly multiple received frames can be queued before readback by the SOC host controller, and optionally trigger a programmable interrupt upon frame receipt. FIFO status can be monitored by the SOC host controller. The FIFOs can be register based for true compatibility with all backend flows, or can be implemented using vendor specific macros (such as Altera LPMs or Xilinx CoreGen components).

Error detection is provided through a CRC. The CRC division polynomial is

$$P(X) = X^8 + X^4 + X^3 + X^2 + 1$$

The data frame is shifted through the CRC circuit on the transmission side, producing a CRC byte which is appended to the end of the frame. The receiver shifts the incoming frame, including the CRC byte, through the CRC circuit and this CRC checker will always output 0xC4 if the CRC passes, regardless of frame content.

To assist in generation of the synchronous j1850 clock tick frequency a fractional clock generation RTL circuit can be provided to produce: fractional clock generation RTL circuit can be provided to produce:

$$F_{out} = F_{in} \times \frac{N}{2^k}$$

where

$$F_{out} \leq \frac{1}{2} \times F_{in}$$

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Resource Utilization

The J1850 core is not limited to any vendor specific implementation. Versions are available for all major FPGA vendors, and can be created for any custom ASIC application. The following tables show typical resource requirements for an Altera implementation.

Design	J1850 Core
LC's (Includes FF's)	1537
FF's	936
Mem Bits	4104
M4Ks	3

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