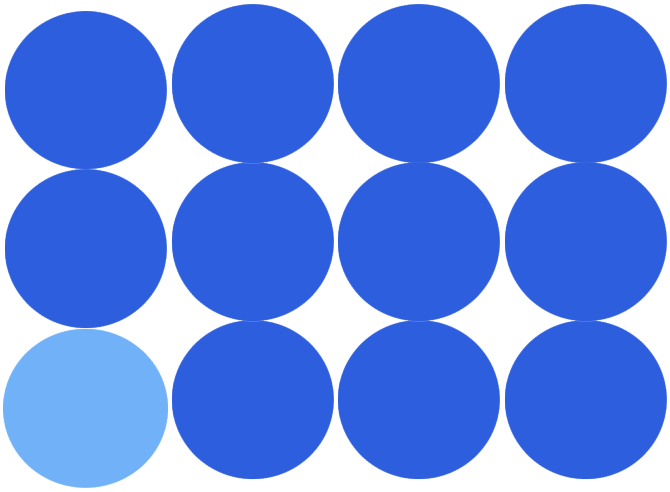
I2C Core Datasheet



The I2C core is a full featured core that is compliant with the I2C 2.1 Specification.

Features

- I2C 2.1 Compliant
- Operates in Master, Slave, or Multi-Master modes.
- Operates in Fast (400kHz) or Standard (100kHz) modes.
- Easy to use command structure
- Simple local bus access to all configuration registers and FIFOs.
- Programmable Interrupt Controller
  - Enable
  - Mask
  - Status
- Software driver and example support

General Information

The I2C core is capable of operating in master, slave, or multi-master modes. Both Fast (400kHz) and Standard (100kHz) modes are supported.

The design is fully synchronous to a single system clock input, and has an asynchronous active low system reset.

The I2C core has been designed to allow for easy integration into custom user applications. The user application can read or write control/data registers using a simple control interface. Versions also exist that communicate with the OPB in Xilinx PPC implementations.

This I2C core is built with optimal system performance in mind. The buffer size is scaleable and capable of holding multiple transactions. This improves system performance by allowing high speed bursting of data to the I2C interface. Software can perform other tasks while the I2C core handles the slower speed accesses to the device.

In Master Mode, software can load the Master TX FIFO with multiple transactions, then simply write the GO bit of the I2C_CONTROL register. The I2C Core will process all transactions in the queue and give interrupt notification when the operation completes. For reads, software can retrieve data from the Master RX FIFO.

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More General Information

In Slave Mode, the I2C Core can provide information to the requesting Master. If the implementation has a local processor, an interrupt can be generated that will notify the local processor of the Slave access. The local processor then has the ability to see what was accessed by checking the Slave Write History FIFO, and can respond accordingly if need be.

Facilities are also in place to monitor all buffer levels, flush buffers, define the I2C chip address, soft reset the core, specify the maximum number of retries, and monitor the actual number of retries.

A fully functional Interrupt Controller is provided with enable control and status for each interrupt.

I2C Interface

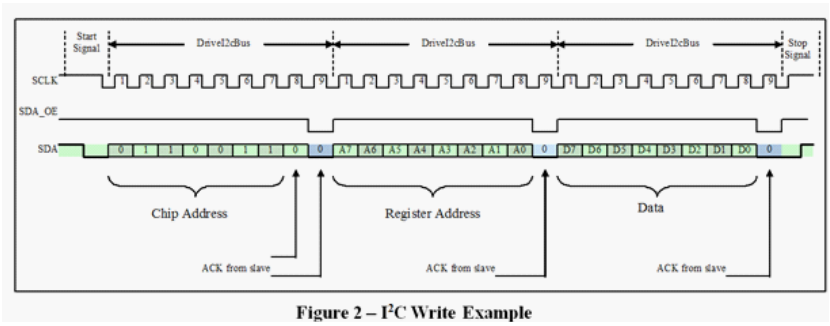
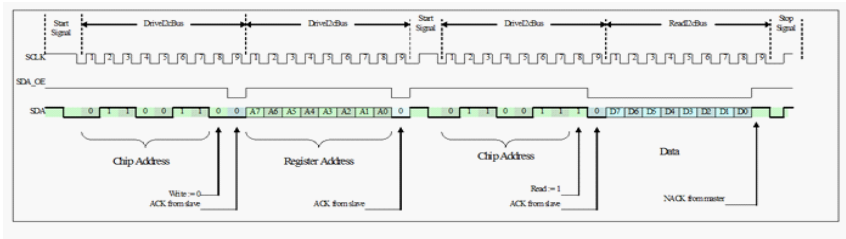
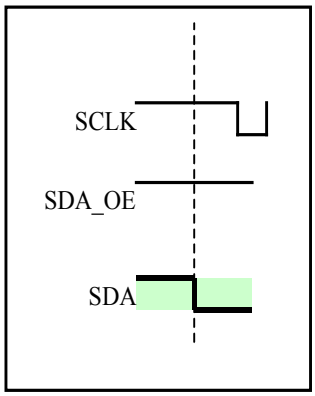


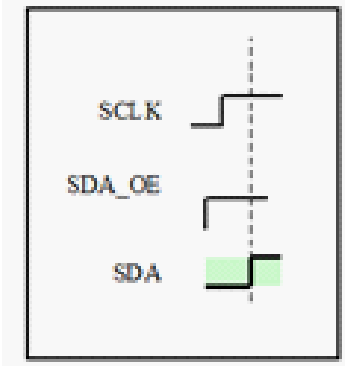
Figure 2 – I²C Write Example



I2C Interface



I²C Start



I²C Stop

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