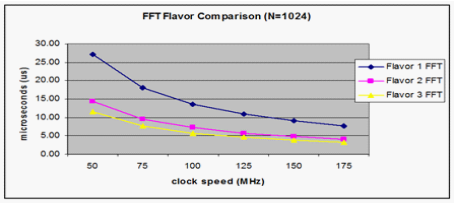
High Speed FFT Datasheet

The FFT core is full featured core that implements a programmable depth (N) complex FFT.

Features

- FFT or IFFT
- Very high speed
- Programmable N
- N-point complex FFT or 2N point real FFT
- Hardware efficient
- Floating point and block floating point versions
- Versions capable of arbitrary internal precision
- Radix-2 DIT (decimation in time) algorithm with proprietary speed enhancement techniques



General Information

It uses a proprietary architecture which results in extremely fast implementations, realizable in most technologies, very portable, and expandable and parameterizable for a multitude of applications. The clock speeds required are practical, and the design has is field proven. Three flavors exist, and their performance is outlined below.

FPGA Resources

(For 18 bit multiplier, 22 bit internal precision, block floating point versions)

	Flavor 1 (fast)	Flavor 2 (faster)	Flavor 3 (fastest)
Slices*	3500	7000	10000
LUTs*	2000	4000	6000
FFs*	4000	8000	10000
Multipliers	16	32	48
BRAMs	24	48	48

*Estimates for Vitex II or equivalent, depends on packing

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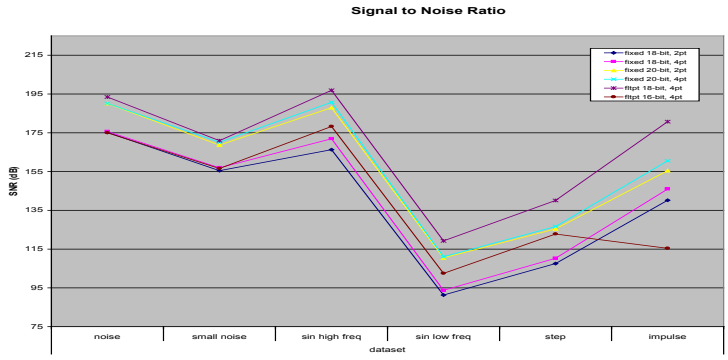
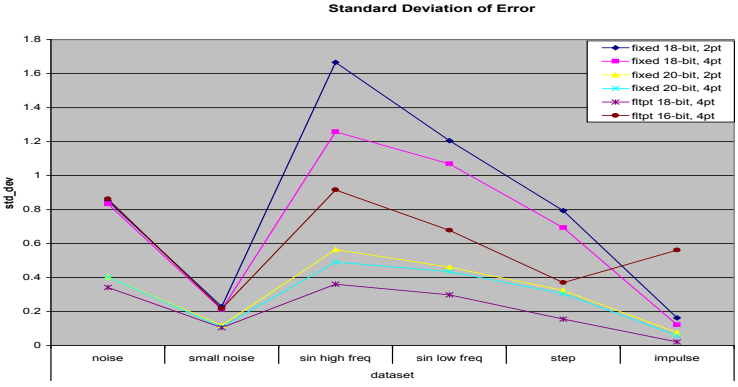
High Speed FFT Design

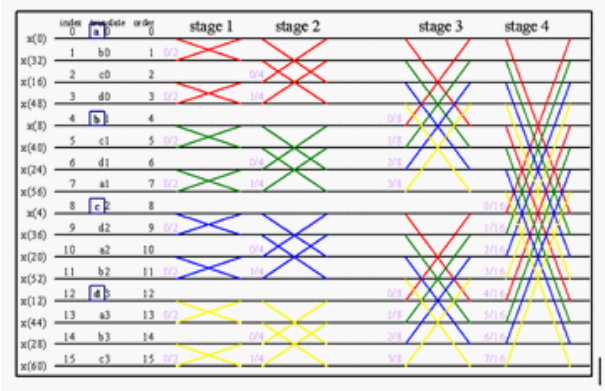
The following plots reflect the performance of a system which was comprised of the 1024-point complex FFT, a filter, and a 1024 point complex IFFT, to implement a convolution function (i.e. frequency domain filter). The input data was 16 bits, the filter coefficients were 18 bits, and the clock speed was 125MHz. Several types of signals were analyzed, as indicated on the x-axis. Contact DDC for details on floating point versions, and versions with higher resolutions. Several versions exist with higher precisions.





Applications

- Video/Imaging
- Convolution
- Frequency Domain Filtering
- Spectral Analysis
- Power Spectral Density
- Communications



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