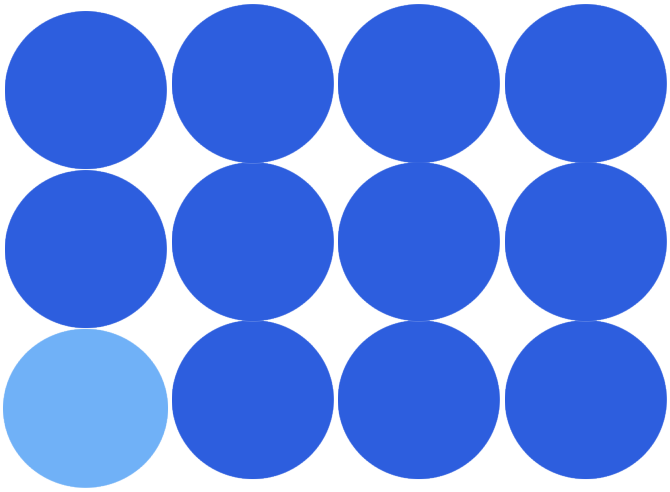
DDR/DDR2 Controller Datasheet



Design Package File

The design package file for the controller can be modified to support various parameters such as row, column, bank address bits widths, local bus width (always twice as wide as the physical DDR/DDR2 data path to the memory devices), along with timing related settings for the general operation of the core. In addition the number of read/write ports and relative priority of each port can be configured. The core contains the following modules:

N x Read port

M x Write port

Command Arbiter

SD Control Core

DDR IO

The DDR/DDR2 Multi-channel Memory Controller core is a full featured core that is compatible with industry standard DDR and DDR2 memory devices with appropriate settings.

General Information

The controller must be configured for at least one read port and one write port. There is no implicit limit on the number of read or write ports and the number of read and write ports does not need to be balanced thus make this core ideal for many high end video processing applications.

To ease system timing requirements and interface coding the SDRAM controller supports write data/command interfaces operating at a different frequency to the DDR core memory clock (and independent of each other) effectively allowing many different slower (or faster if necessary) write paths to memory. In the same manner the controller supports read command ports running at different frequencies to core and independent to each other. However the read data path for each read port is supplied data at the full wide rate and it is up to the particular read process to properly size an external FIFO. This allows the minimum system requirements to be implemented since each read process is aware of its own buffering requirements.

Digital Design Corporation

Digital Design Corporation • 3820 Ventura Dr. Arlington Hts. IL 60004 • Phone: 847-359-3828 • Fax: 847-359-5418
Website: www.digidescorp.com • E-Mail: sales@digidescorp.com

Controller Diagram

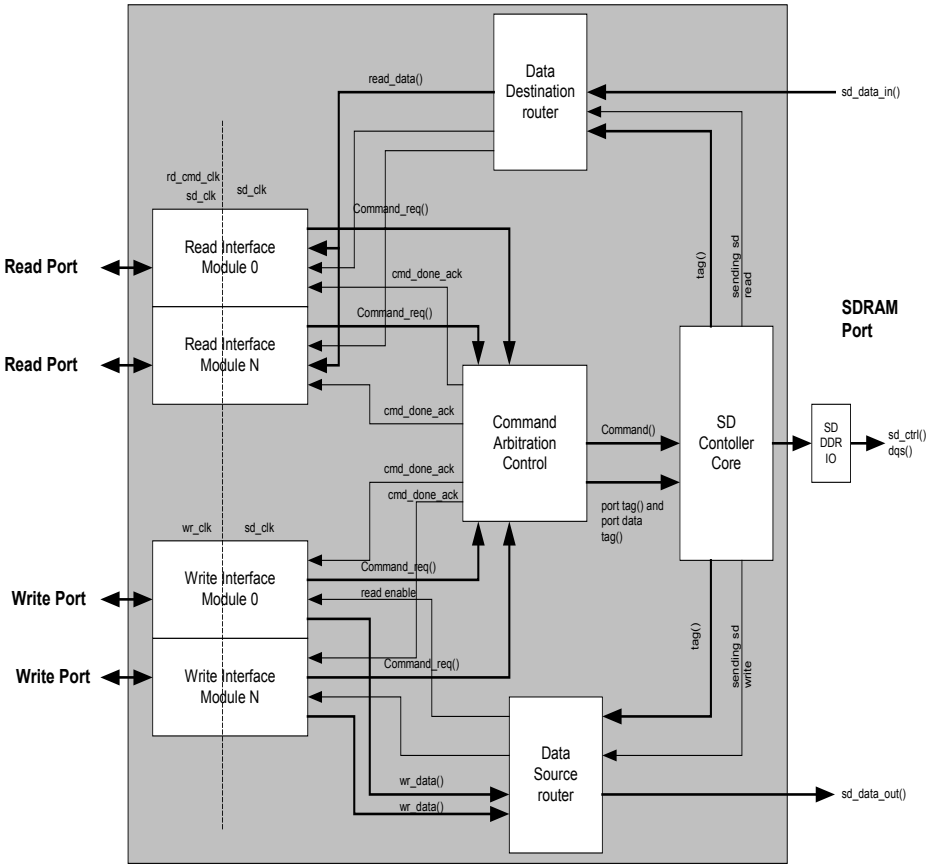


Figure 1. Top Level Diagram

Table 1. Speed/Size Breakdown

Synthesis Option	Approx Altera Atoms/ESBs	Approx Xilinx Slices/ BMEM	Approximate Speed (non-optimized)
1 read, 1 write port		~1200 SLices 4 BRAMs	Xilinx Virtex II -6, ~133 MHz Without floor planning
Each additional read port		200 Slices, 2 BRAMs	
Each additional write port		200 Slices, 2 BRAMs	

Feature Summary

- DDR/DDR2 support (defined in package file)
- Multi Channels (M x read, N x write) through generic settings. Each port can have an independent clock (up to the limits of the host FPGA/ASIC)
- Local Data path width is 2x the memory physical width
- Port and timing parameters configurable in a package file
- Byte enables are supported on each write port
- Built in handing of misaligned transfers when using DDR2 (4n prefetch) memory
- Support for independent clocks for each read command and write data/command port.
- Priority setting for each port allows more memory bandwidth to be allocated for certain channels as needed by the application
- Smart Burst © port operation. Write data can trickle in and the controller will optimize when to burst the stored data to memory. Internal burst size preference can be set for each port. Write timeout is settable via generics.
- Data tags are supported on each read port to allow identification of returning read data.

3820 Ventura Dr.
Arlington Heights IL, 60004
Phone: 847-359-3828
Fax: 847-359-5418
www.digidescorp.com
Email: sales@digidescorp.com

For more information contact Digital Design Corporation sales at:

+ 1-847-359-3828

or go to our website at:

www.digidescorp.com

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