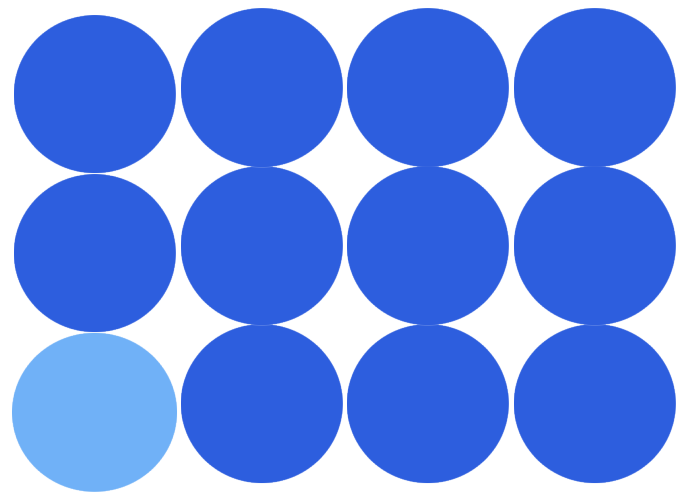


CAN 2.0 Network Controller Core



Properties

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed realtime control with a high level of security. Largely employed in automotive electronics, CAN is employed in applications ranging from high speed networks to low cost multiplex wiring.

- prioritization of messages
- guarantee of latency times
- configuration flexibility
- multicast reception with time synchronization
- system wide data consistency
- multi-master
- error detection and signaling
- automatic retransmission of corrupted messages as soon as the bus is idle again
- distinction between temporary errors and permanent failures of nodes and autonomous switching off of defect nodes

The CAN 2.0 Network Controller core is an ISO 11898 compliant Controller Area Network (CAN) stand-alone controller.

General Information

The CAN core provides an interface between a microprocessor and a CAN bus; implementing all of the data encoding/decoding, message management and buffering, bit timing and re-synchronization required to transmit and receive data over a CAN network. When connected to external CAN compliant transceivers the CAN core supports programmable bus speeds up to 1 Mbps. The CAN core is modeled after the industry standard Philips SJA1000 when operating in PeliCAN mode. Existing software drivers for the SJA1000 may be easily integrated.

Resource Utilization

The CAN 2.0 Network Controller core is not limited to any vendor specific implementation. Versions are available for all major FPGA vendors, and can be created for any custom ASIC application. The following tables show typical resource requirements for an Altera implementation.

Design	LCs (includes FFs)	FFs	Mem Bits	M4Ks
CAN Controller	2567	1494	1280	2



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Functional Description

The external CPU accesses the CAN core through a generic micro-processor interface (address, data, control, interrupt). All internal registers and data buffers are provided through this interface. The register map and bit definitions are modeled after the SJA1000 standalone controller. Messages to be transmitted are written by the CPU to the transmit buffer. When commanded by the CPU the CAN core handles all aspects of the transmission, generating a programmable interrupt on completion or failure. Messages received by the core are placed in the receive buffer. The receive buffer is a 64 byte circular buffer, allowing up to 5 extended frame messages to be received without CPU intervention. As the CPU reads each message that buffer space is made available for more incoming data. If the buffer is empty, the first received message can generate a programmable interrupt. Received messages are first compared against the acceptance filter. Only messages meeting the acceptance criteria of the filter are placed in the message buffer. In this way traffic not intended for this node is filtered out without CPU intervention.

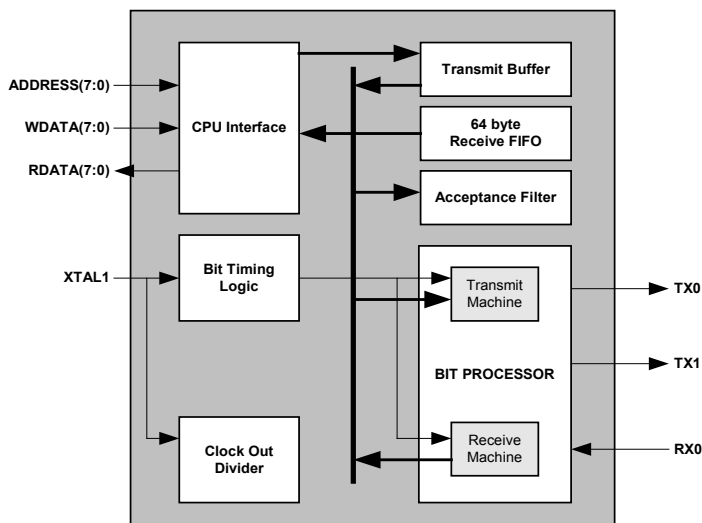
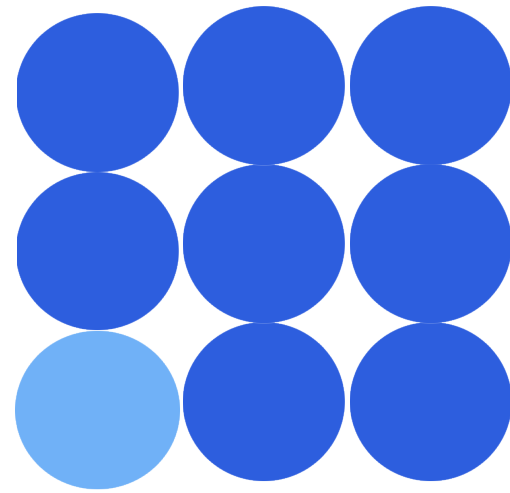


Figure 1 - CAN Interface Block Diagram



Feature Summary

- Supports full CAN 2.0 (both parts A and B)
- Supports 11 bit and 29 bit identifiers
- Data rates up to 1 Mb/s with support for slower standard bus speeds
- Buffered CPU access with multi-message receive buffer (64 bytes)
- Robust CAN bus error detection and reporting
- Flexible Acceptance Filtering
- Listen-Only, Self-Reception, and Self-Test modes
- Read/Write error counters
- Programmable interrupt controller
- Modeled after industry standard SJA1000
- Fully synchronous design
- Standard IPIF/OPB bus interface wrapper available
- VHDL Test bench available for verification and example of operation

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