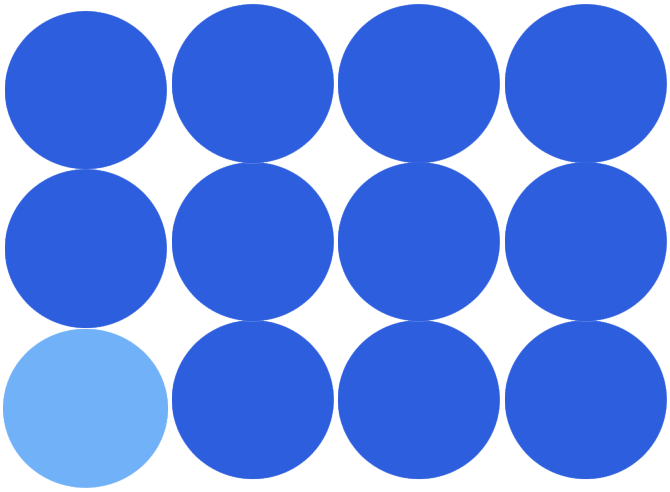
The 1553B Core Datasheet



Bus Controller Features

- BC to RT RX transaction control.
- BC to RT TX transaction control.
- RT to RT transaction control.
- Broadcast command generation.
- Generation of all Mode commands.
- Transaction list generation.
- Command and Status FIFO with 4KB Data Memory.
- Dual redundant communication (A/B) with an upgrade path to more redundant channels.
- Error detection and status reporting for all transactions.
- Programmable no response timeout.
- Programmable automatic retry logic.
- Programmable interrupt.
- Terminal failsafe protection.
- On the fly loopback check.

The 1553B core is a full featured core that is compliant with the Department of Defense MIL-STD-1553B specification.

The 1553B Core

The design package consists of a core that contains the "1553B" data specific functions for the general operation of the core. A 1553B behavioral model and simulation environment is also provided to the designer for simulation/verification of the 1553B design in the system. Software driver-examples and support are available to accelerate application development.

Resource Utilization

The following resource numbers are presented for various Xilinx devices. These numbers do not include the BusProbe option. BusProbe is an debug feature that will allow the user to trace and monitor various processing states and signals for purposes of debugging an implementation. BusProbe adds about 10% to the size of the design. It is recommended for first implementations and can be removed from final versions, to conserve chip resources, by a simple flip of a generic switch. Switching between BC only, RT only, BM only, implementing all three, or any combination of two, is also done by a simple flip of a generic switch.

Table 3 – Virtex4

Capability	Slices	Flops	LUTs	16k x 1 BRAM
BC/RT/BM	2749	1974	4638	26
BC only	1111	886	1836	7
RT only	1898	1430	3241	12
BM only	1002	664	1668	11

Table 4 – Virtex5

Capability	Slices	Flops	LUTs	16k x 1 BRAM
BC/RT/BM	1663	1970	3827	26
BC only	548	884	1541	7
RT only	1009	1426	2623	12
BM only	561	665	1426	11

Table 5 – Virtex6

Capability	Slices	Flops	LUTs	16k x 1 BRAM
BC/RT/BM	1383	1959	4341	26
BC only	617	898	1742	7
RT only	1000	1413	3039	12
BM only	458	691	1525	11

Table 6 – Spartan6

Capability	Slices	Flops	LUTs	16k x 1 BRAM
BC/RT/BM	1519	1959	4406	26
BC only	643	898	1746	7
RT only	1062	1413	3138	12
BM only	450	691	1532	11

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The 1553B Core Design

The 1553B Interface Core is comprised of several blocks which are shown in the following block diagram. All signals on the bottom go to the user application. All signals on the left go to the 1553B Tranceiver.

The 1553B core has been designed to allow for easy integration into custom user applications. A standard processor bus interface is provided to access control/status registers, FIFOs, and RAMs. The standard version supports a 32 bit user bus width but can be delivered with any byte width needed in the user application. Fully customized interfaces are available.

A programmable interrupt controller is included with full enable, masking, and status capability to allow for interrupt driven or polled detection of events.

The 1553B core contains the following three major functions.

1. Bus Controller (BC)
2. Remote Terminal (RT)
3. Bus Monitor (BM)

These functions can be used independently, or in conjunction based on the users needs. The design is capable of switching from BC to RT mode and back, on the fly. To support 1553 communication, the BC, RT, and BM share one Manchester II Differential Encoder, and two Manchester II Differential Decoders.

Detailed operation of the design is provided in the User Guide.

Remote Terminal Features

- Programmable RT address (0-30) via pins with software programmable override.
- Supports 30 simultaneous RX sub-addresses (1-30).
- Supports 30 simultaneous TX sub-addresses (1-30).
- Supports independent 32 word buffers for each TX and RX sub-address. All data buffers are double buffered to avoid data corruption and allow higher throughput.
- Broadcast command reception.
- Supports all Mode commands and automatically handles relevant Mode commands in hardware.
- 512 deep message queue with filtering.
- Programmable status response.
- Programmable response time.
- Programmable interrupts
- Programmable command legalization table per sub-address with entries for broadcast, transmit/receive/both, and any number of word count combinations.
- Programmable Mode command legalization.
- Error detection and reporting with automatic handling in hardware.
- On the fly loopback check.
- Instrumentation support.
- Sub-address 30 automatic wrap-around mode with wrap rejection logic.
- Automatic switching to the redundant bus on reception of a simultaneous new command.
- Dual redundant communication (A/B) with an upgrade path to more redundant channels.

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