



General Description:

The VME core is conforms to the VME standard ANSI/VITA 1-1994 for VME 64 and to the VME standard ANSI/VITA 1-1997 for VME 64x. The modular design allows integration of only the necessary functions.

It also only supports the minimum specification of VME64x, none of the extended functionality has been included.

A VME behavioral model and simulation environment is also available for simulation/verification of the VME design in the system.

Software driver examples and support are available to accelerate application development.

Feature Summary:

- VME Master with requestor
- VME Slave
- VME Bus Timer
- VME Bus Arbitrator
- VME System Controller
- VME Interrupt Handler.
- Supports the D08, D16, D32 and D64 data modes.
- Supports A16, A24 and A32 address modes
- Supports Read, Write, Block Transfers, Multiplexed Block Transfers, Read-Modify-Write, Address Only with Handshaking and Lock cycles
- Memory Mapped Access
- Master DMA Transfers

Resources:

The VME Core is not limited to any vendor specific implementation. Versions are available for all major FPGA vendors and can be created for any custom ASIC application. The following tables show typical resource requirements for a Xilinx implementation

Table 1– VME Core Resources

Module	Slices	16k x 1 Block RAMs
Master	998	1
Slave	660	0
Registers	844	0
Timer, Arbitrator and Interrupt Handler	156	0

*Estimates for Virtex II or equivalent, depends on packing

Core Design

The VME Interface Core is comprised of several blocks which are shown in the following block diagram. The VME core has been designed to allow for easy integration into custom user applications. The VME Core contains the following functions, VME Master, VME Slave, VME Bus Timer, VME Bus Arbitrator, VME System Controller and VME Interrupt Handler. The VME master and VME slave modules share access to the internal processor bus.

The VME Master has two modes of operation. The VME accesses can be coupled or DMA'ed. During coupled operations, the VME master will stall the internal bus until the VME transfer is complete. Read-Modify-Write cycles can only operate in coupled mode.

Interrupts

There are two internal interrupt outputs from the VME Core, a high priority and a low priority. Each of the potential interrupt sources can be independently enabled on either interrupt.

Interrupt Sources

- VME IRQ1-7
- Master Transaction Complete
- Master DMA Complete
- Master RMW Complete
- Slave Transaction Complete
- VME BERR
- VME SYSFAIL
- VME SYSRESET
- VME AC FAIL

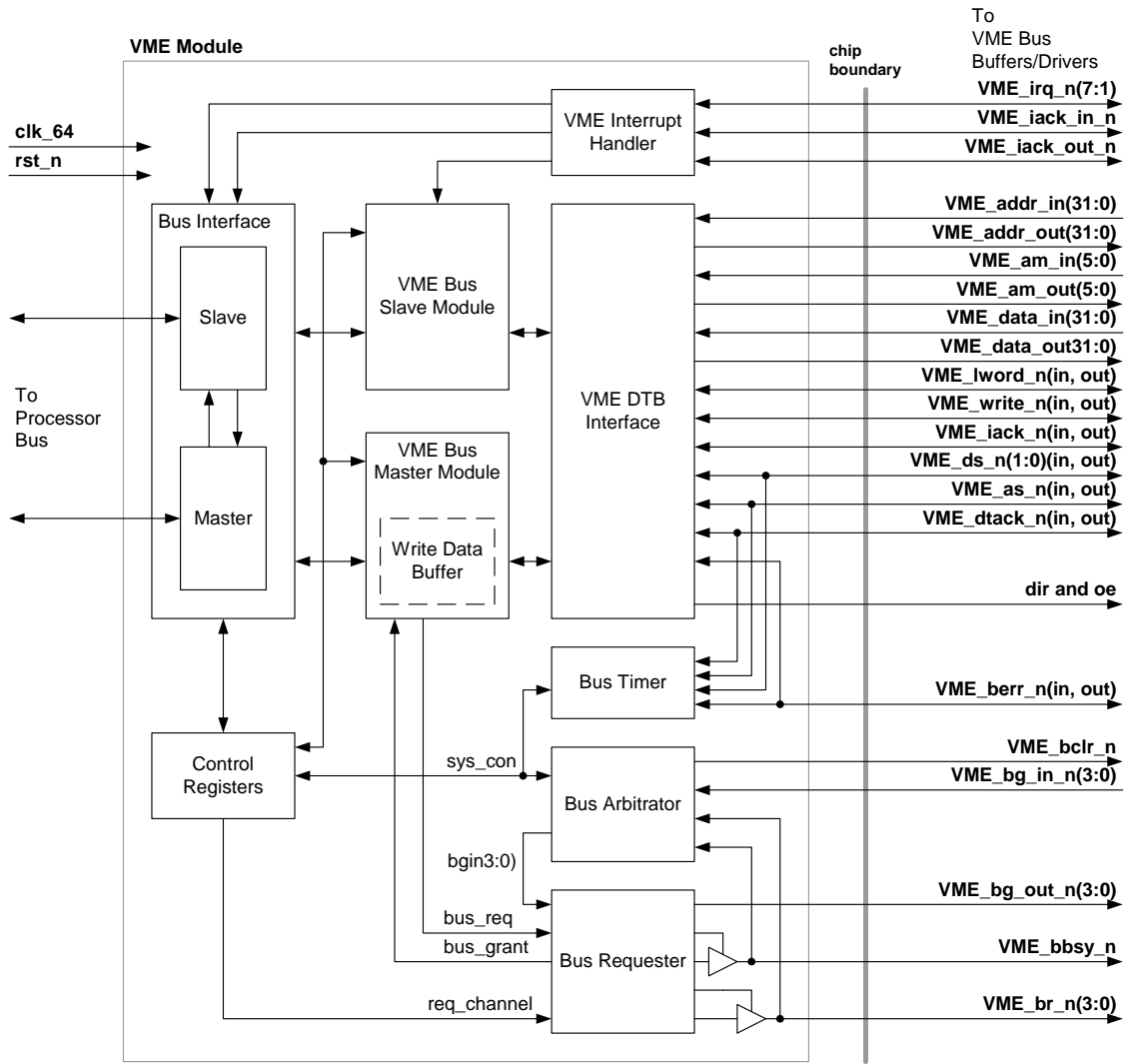


Figure 1 – VME Core Diagram

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Table 2 – VME Core I/O

Signal Name	Width	Dir	Signal Description
System			
clk_64	1	I	64 MHz system clock
rst_n	1	I	Asynchronous chip reset (active low)
VME Outputs			
VME_br_out_n	4	O	VME Bus Request Output for master
VME_bgout_n	4	O	VME Output Bus Grant
VME_irq_out	7	O	VME Interrupt Request Output.
VME_sys_fail_out_n	1	O	VME System Failure Output.
VME_sysreset_out_n	1	O	VME System Reset Output
VME_bbsy_out_n	1	O	VME Bus Busy Output.
VME_berr_out_n	1	O	VME Output Bus Error.
VME_ac_fail_out_n	1	O	VME AC Failure Output
VME_iackout_n	1	O	VME Interrupt Acknowledge Output
VME Inputs			
VME_br_in_n	4	I	VME Bus Request Input for arbitrator
VME_bgin_n	4	I	VME Bus Grant Input
VME_irq_in	7	I	VME Interrupt Request Input
VME_sys_ail_in_n	1	I	VME System Failure Input
VME_sysreset_in_n	1	I	VME System Reset Input
VME_bbsy_in_n	1	I	VME Bus Busy Input
VME_berr_in_n	1	I	VME Bus Error Input
VME_ac_fail_in_n	1	I	VME AC Failure Input
VME_iackin_n	1	I	VME Interrupt Acknowledge Input.
VME_bclr_n	1	I	VME Bus Clear Input
VME Bi-Directional Signals			
VME_a_I	32	I	32-bit VME Input Address Bus
VME_a_O	32	O	32-bit VME Output Address Bus
VME_a_T	1	O	VME Address Bus Tri-state Control
VME_am_I	6	I	6-bit VME Input Address Modifier Bus
VME_am_O	6	O	6-bit VME Output Address Modifier Bus
VME_am_T	1	O	VME Address Modifier Tri-state Control
VME_d_I	32	I	32-bit VME Input Data Bus
VME_d_O	32	O	32-bit VME Output Data Bus
VME_d_T	1	O	VME Data Bus Tri-state Control
VME_ds_n_I	2	I	VME Data Strobe 0 and 1 Inputs
VME_ds_n_O	2	O	VME Data Strobe 0 and 1 Outputs
VME_ds_T	1	O	VME Data Strobe Tri-state Control
VME_dtack_n_I	1	I	VME Data Acknowledge Input
VME_dtack_n_O	1	O	VME Data Acknowledge Output.
VME_lword_n_I	1	I	VME Long Word Control Bit Input
VME_lword_n_O	1	O	VME Long Word Control Bit Output.

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Signal Name	Width	Dir	Signal Description
VME_lword_T	1	O	VME Long Word Control Bit Tri-state Control
VME_write_n_I	1	I	VME Write Input
VME_write_n_O	1	O	VME Write Output
VME_write_T	1	O	VME Write Output Tri-state Control
VME_iack_n_I	1	I	VME Interrupt Acknowledge Input.
VME_iack_n_O	1	O	VME Interrupt Acknowledge.
VME_as_n_I	1	I	VME Address Strobe Input
VME_as_n_O	1	O	VME Address Strobe Output
VME_as_T	1	O	VME Address Strobe Tri-state Control
VME Output Enables and Direction Control			
VME_addrs_dir	1	O	VME Address Direction Control
VME_data_dir	1	O	VME Data Bus Direction Control
VME_vam_dir	1	O	VME AM Direction Control
VME_con_dir	1	O	VME Direction Control
VME_ds_dir	1	O	VME Data Strobe Direction Control
VME_as_dir	1	O	VME Address Strobe Direction Control
VME_slave_dir	1	O	VME Slave Direction Control
VME_oe	1	O	VME Output Enable

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